S Number	Hits	Search Text	DB	Time stamp
1	26618	point adj point	USPAT; US-PGPUB	2002/01/04 15:00
2	12595	memory adj controller	USPAT; US-PGPUB	2002/01/04 15:13
3	19	(point adj point) with (memory adj controller)	USPAT; US-PGPUB	2002/01/04 15:00
4	30622	memory adj control$4	USPAT; US-PGPUB	2002/01/04 15:14
5	24	(point adj point) with (memory adj control$4)	USPAT; US-PGPUB	2002/01/04 15:15
6	5	((point adj point) with (memory adj control$4)) not ((point adj point) with (memory adj controller))	USPAT; US-PGPUB	2002/01/04 15:15

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DOCUMENT-IDENTIFIER: US 4977498 A
TITLE: Data processing system having a data memory interlock coherency scheme

BSPR:
Generally, the present invention comprises a memory system coupled, by a bus arrangement, to an Input/Output (hereinafter "I/O") adapter module. The memory system is also coupled, by a point to point bus arrangement, to multiple central processing units (hereinafter "CPUs"), and is thereby shared between such CPUs. Furthermore, the memory system includes a central memory controller, to which the CPUs and I/O adapter are coupled. The memory controller is coupled, by a point to point bus arrangement, to a plurality of memory modules, while the I/O adapter is coupled, by a bus arrangement, to I/O devices or other memory systems. The I/O adapter and each CPU has a cache memory.